MULTILAYERED SUBSTRATE WITH BUILT-IN ELECTRONIC COMPONENT

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Priority number(s): JP20030075977 20030319

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Abstract of **JP2004288711**

PROBLEM TO BE SOLVED: To provide a multilayered substrate with a built-in electronic component having a highly reliable connection structure in which no crack occurs from the contacts between the edges of transition layers and passivation layers and, in addition, no treating liquid enters into the interfaces between die pads and a resin layer through the wall surfaces of bumps.
SOLUTION: This multilayered substrate 21 with the built-in electronic component is provided with an electronic component 25 embedded in the resin layer, transition layers 29 formed on the pads 27 of the component 25, and passivation films 28 covering the pads 27. This substrate 21 is also provided with via holes 31 formed on the transition layers 29 and wiring layers 32 connected to the transition layers 29 through the via holes 31. The diameters (Dd) of the transition layers 29 are made smaller than those (De) of the pads 27 and larger than the diameters (Df) of the openings of the passivation films 28 covering the pads 27.
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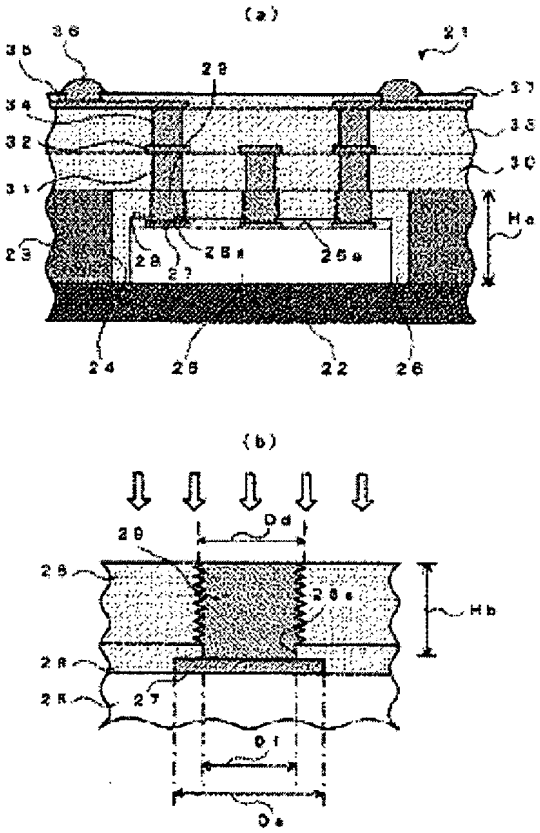

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]
Especially this invention relates to the electronic-parts built-in multilayer substrate having the electronic parts in which the transition layer of an arbitration height dimension was formed on the die pad, about an electronic-parts built-in multilayer substrate.
[0002]
[Description of the Prior Art]
an electronic-parts built-in multilayer substrate -- the interior of a multilayer printed wiring board -- electronic parts, such as a semiconductor integrated circuit (it abbreviates to "IC" below.) chip, -- "laying under the ground" (on these specifications, it is expressed as "built-in" for convenience.) -- making -- things are said although constituted. Between electronic parts and a printed wired board, since the Bahia hall etc. connects directly, the members for connection (a wire, a lead, or bump) in the mounting approaches, such as wire bonding, and TAB (Tape Automated Bonding) or a flip chip, are not needed, for example. Therefore, various faults (an open circuit, a poor contact, or corrosion) which coil round those members for connection are not produced, and high dependability is acquired.
[0003]
<1st conventional example:, for example, patent reference 1 reference,>
Drawing 7 is the 1st sectional view (a) and its important section expanded sectional view (b) of the conventional example. In these drawings the electronic-parts built-in multilayer substrate 1 It is the crevice (it is also only called a hollow or a cavity.) which had the multilayer structure of one or more layers, for example, a three-tiered structure, and the arbitration layer (drawing the 1st layer) carried out the laminating of the core substrate 3 which has the predetermined thickness dimension Ha on the heat sink plate 2 which used aluminum etc., and was formed at the core substrate 3. After putting electronic parts 5 into 4 and fixing between the base of the electronic parts 5, and the heat sink plates 2 with adhesives, insulating resin 6 is filled up with and closed in the clearance between crevices 4.
[0004]
While electronic parts 5 have the electrode (henceforth a "die pad") 7 of the number of arbitration (for convenience [by a diagram] three pieces) formed in the top-face 5a, here It has the passivation film 8 which covered this top-face 5a and was formed. Hole 8a is opened in the passivation film 8 so that a part of each front face of a die pad 7 may be exposed, and it has the transition layer 9 of the predetermined height dimension Hb which connects with a die pad 7 electrically through the hole 8a. Small section 9a which has the opening dimension Da of hole 8a and the width method of abbreviation equivalence for the ability to have opened the transition layer 9 in the passivation film 8 in a detail more, It consists of large section 9b which has the larger width method Dc which follows the upper part of the small section 9a than the width method Db of a die pad 7, and the height dimension of the whole which doubled such small section 9a and large section 9b is set to Hb. In addition, in order to raise bonding strength with insulating resin 6, roughening processing is carried out, and the front face of the transition layer 9 has

shown the processing side where roughening processing was performed with the serrate wavy line in the example of illustration.
[0005]
The transition layer 9 is formed for right conductivity materials, such as copper, and the diameter size method (however, the breadth dimension when carrying out a right pair to a drawing: Dc) of the transition layer 9 is set up more greatly (Dc>Da) than the diameter of opening of hole 8a formed on the die pad 7 (Da). This is clear also from the publication of the drawing (especially Fig. 6) of this bibliography 1, and the publication (" between which the transition layer of a big path is made to be especially placed by the pad top of "IC chip) of the paragraph [0037] of this bibliography 1.
[0006]
And the electronic-parts built-in multilayer substrate 1 of illustration the 1st layer top which has such structure -- the insulating layer 10 of a predetermined thickness dimension -- a laminating -- carrying out -- the insulating layer 10 -- the Bahia hall 11 of a required number, and the conductor of a necessary configuration -- a circuit 12 -- forming -- a two-layer eye and nothing -- furthermore, the two-layer eye top -- the insulating layer 13 of a predetermined thickness dimension -- further -- a laminating -- carrying out -- the insulating layer 13 -- the Bahia hall 14 of a required number, and the conductor of a necessary configuration -- a circuit 15 -- forming -- the 3rd layer and nothing -- and the conductor of the maximum upper layer -- the solder bump 16 for connecting with external substrates, such as a DOTA board, is formed in a circuit 15, and the coat of the whole maximum upper front face except those solder bumps' 16 formation part is carried out by the insulator layer 17, and it is constituted.
[0007]
<2nd conventional example:, for example, patent reference 2 reference,>
as the 2nd conventional example -- the diameter size method of the transition layer 9 -- what is set to (diameter (Da of opening of hole 8a formed on the die pad 7 in Dc) "the above") is known. Specifically, it is specified "the width of face of a transition layer is 1.0 to 30 times the width of face of a pad" as indicated by "claim 2" of this bibliography 2. If its attention is paid to "1.0" of numerical limitation of this convention, since it will be "1.0 times" the width of face of the width-of-face = pad of a transition layer, this means making into equivalence (Dc=Da) the diameter of opening (Da) of the diameter size method (Dc) of the transition layer 9 in the 1st above-mentioned conventional example, and hole 8a formed on the die pad 7.
[0008]
<3rd conventional example:, for example, patent reference 3 reference,>
The technique fill [technique] up a crevice with insulating resin, embed [technique] a semiconductor chip, carry out [technique] a perforating process with laser etc., and it was made to expose a stud bump's head for the 3rd conventional example from a resin layer after forming the stud bump in the bonding pad formed in the semiconductor chip and mounting the semiconductor chip in the crevice of a printed circuit board is indicated.
[0009]
[Patent reference 1]
JP,2001-339165,A ([0017]-[0019], [0037], Fig. 6)
[Patent reference 2]
JP,2001-352174,A [claim 2]
[Patent reference 3]
The patent No. 2842378 official report ([0016]-[0020], Fig. 1st [the] and 3)
[0010]
[Problem(s) to be Solved by the Invention]
however, above-mentioned the 1- the following troubles are held if it is in the 3rd conventional example.

(1) In the 1st conventional example, since it is transition layer (path Dc) > putt (path Da), when it is easy to produce a crack with the contact of the edge of a transition layer, and a passivation layer as the starting point, this crack passes passivation and a semi-conductor substrate is reached, there is a trouble

that the damage to a die occurs.
(2) In the 2nd conventional example, although it is transition layer (path Dc) >= putt (path Da) and especially a damage [as opposed to a die at the conditions of Dc=Da] is not generated, it is very difficult to form a transition layer and putt by the same width of face, and there is a trouble of not being practical.
(3) In the 3rd conventional example, since die putt parts other than a bump loading field (die putt part with high display flatness) will touch a resin layer, processing liquid tends to invade into the interface of die putt and a resin layer through a bump's wall surface at the time of plating or DESUMIA processing, and there is a problem that exfoliation arises.
[0011]
Therefore, the thing which a crack produces especially the purpose of this invention among the above-mentioned troubles with the contact of the edge of a transition layer, and a passivation layer as the starting point, and a die damage generates, And the thing which processing liquid invades into the interface of die putt and a resin layer through a bump's wall surface, and exfoliation produces Both are new knowledge and it is in offering the electronic-parts built-in multilayer substrate which pays its attention for being described by any advanced technology and twisting, and solves these technical problems to coincidence, with has reliable connection structure.
[0012]
[Means for Solving the Problem]
The electronic parts laid under the resin layer in order that this invention might attain the above-mentioned purpose, The transition layer formed on the pad of these electronic parts, and the passivation film which covers said pad, In the electronic-parts built-in substrate possessing the Bahia hall formed on said transition layer, and the wiring layer connected to said transition layer through this Bahia hall It is characterized by setting up more greatly [in the path of said transition layer, it is smaller than the path of said pad, and] than the diameter of opening of the passivation film which covers said pad.
In this invention, since the path of a transition layer is set up more greatly than the diameter of opening of the passivation film which covers the periphery of a pad smaller than the path of a pad, the angle of a transition layer is not located on a pad. For this reason, even if the passivation film is under a transition layer, it will not be concerned with stress (force generated in the time of a resin press etc.) from a top, but the crack initiation of the passivation film and the structural members (Si etc.) under it will be avoided.
[0013]
[Embodiment of the Invention]
Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. Drawing 1 is the sectional view (a) and its important section expanded sectional view (b) of the electronic-parts built-in multilayer substrate in the gestalt of operation.
In these drawings, the electronic-parts built-in multilayer substrate 21 has the multilayer structure of one or more layers. the following -- especially -- although not limited -- explanation -- it considers as a three-tiered structure for convenience. The 1st (equivalent to arbitration layer given in summary of invention) layer The laminating of the core substrate 23 which consists of copper which has the predetermined height dimension Ha on the heat sink plate 22 using aluminum etc. is carried out. After putting the electronic parts 25 of arbitration into the crevice (or becoming depressed or cavity) 24 formed in the core substrate 23 and fixing between the base of the electronic parts 25, and the heat sink plates 22 with adhesives, insulating resin 26 is filled up with and closed in the clearance between crevices 24.
[0014]
While the electronic parts 25 in the gestalt of this operation have the die pad (or an electrode or a terminal) 27 of the number of arbitration (for convenience [by a diagram] three pieces) formed in the top-face 25a It has the passivation film 28 which covered this top-face 25a and was formed. Hole 28a is opened in the passivation film 28 so that a part of each front face of a die pad 27 may be exposed, and it has the transition layer 29 formed for right conductivity materials, such as copper of the predetermined

height dimension Hb electrically connected to a die pad 27 through the hole 28a.
[0015]
Covering the whole height, as for the transition layer 29, the width method has the configuration of an abbreviation EQC, and the configuration similar to the alphabetic character of "I" of the alphabet, if it compares and says. Specifically When the height dimension of the transition layer 29 is set to Hb, for example, the width method Dd The whole height dimension Hb is covered. Smaller (De>Dd) than the path De of a die pad 27 And it has the larger (Df<Dd) cross-section configuration of a stock pot mold of in short having De>Dd and the relation of Df<Dd than the opening dimension Df of hole 28a which was able to be opened in the passivation film 28 by being arranged like. Moreover, in order to raise bonding strength with insulating resin 26, roughening processing is carried out, and the front face of the transition layer 29 in the gestalt of this operation has shown the processing side where roughening processing was performed with the serrate wavy line in the example of illustration.
[0016]
The electronic-parts built-in multilayer substrate 21 of illustration on the 1st layer for which it has such structure the insulating layer 30 of a predetermined thickness dimension -- a laminating -- carrying out -- the insulating layer 30 -- the Bahia hall 31 of a required number, and the conductor of a necessary configuration -- a circuit 32 -- forming -- a two-layer eye and nothing -- furthermore, the two-layer eye top -- the insulating layer 33 of a predetermined thickness dimension -- further -- a laminating -- carrying out -- the insulating layer 33 -- the Bahia hall 34 of a required number, and the conductor of a necessary configuration -- a circuit 35 -- forming -- the 3rd layer and nothing -- and the conductor of the maximum upper layer -- the solder bump 36 for connecting with external substrates, such as a DOTA board, is formed in a circuit 35, and the coat of the whole maximum upper front face except those solder bumps' 36 formation part is carried out by the insulator layer 37, and it is constituted.
[0017]
The above-mentioned electronic parts 25 are manufactured according to the following processes. In addition, although the production process of IC chip is made into an example, it is not limited to this here. For example, passive components, such as resistance, a capacitor, and a coil, or they may be included.
< Drawing 2 (a)>
First, a die pad 27 is formed by the well-known approach on a silicon wafer 41. The magnitude of a die pad 27 is De.
< Drawing 2 (b)>
Next, a die pad 27 is covered, the passivation film 28 of predetermined thickness is formed, hole 28a is opened in the passivation film 28, and all the die pads 27 are exposed on it. The opening dimension of hole 28a is Df smaller than the magnitude (De) of a die pad 27.
[0018]
< Drawing 3 (a) - (C)>
Next, the whole passivation film 28 is covered and the resist layer 42 is formed. And the exposure mask 43 which has opening 43a of predetermined magnitude (Dd) is laid on the resist layer 42, exposure and development are performed, and opening 42a is formed in the resist layer 42.
< Drawing 3 (d)>
Next, the transition layer 29 is formed by the bonder or plating into opening 42a of the resist layer 42, and hole 28a of the passivation film 28. Although it can be chosen as arbitration from copper, nickel, gold, silver, zinc, iron, etc., supposing the material of the conductor layer (Bahia hall 31) formed in the upper layer in a back process is copper, as for the material of the transition layer 29, it is desirable to also make the material of the transition layer 29 the same in respect of compatibility (copper).
[0019]
Here, magnitude (Dd) of opening 43a of the exposure mask 43 must be made it is larger than the opening dimension Df of hole 28a formed in the passivation film 28 (Df<Dd), and smaller (De>Dd) than the path De of a die pad 27.
[0020]

< Drawing 4 (a) - (c)>
Next, the remaining resist layers 42 are removed, the transition layer 29 is exposed, the roughening liquid of for example, Meltex CZ8100 grade is sprayed on the exposure 29a, and roughening processing of the exposure 29a concerned is carried out. In addition, when setting the peak to peak of the granularity (irregularity) of roughening processing of exposure 29a to Rz, as for Rz, it is desirable to be referred to as about (preferably Rz= about 0.5-2 micrometers) 0.1-4 micrometers.
< Drawing 5 (a), (b)>
At the last, it cuts in the magnitude of a request of a silicon wafer 41, each fragment is used as electronic parts 25, it is embedded in an arbitration layer (for convenience [in the gestalt of this operation] the 1st layer), and the electronic-parts built-in multilayer substrate 21 of drawing 1 is manufactured.
[0021]
It sets to the electronic-parts built-in multilayer substrate 21 of the gestalt of this operation as above. In the path (Dd) of the transition layer 29, are smaller than the path (De) of a pad 27. And since it was made larger than the diameter of opening of the passivation film 28 (Df), that is, considered as the relation of "De>Dd>Df" Since the force of homogeneity is applied crosswise [of the transition layer 29] even when the welding pressure at the time of carrying out the laminating of the upper layer (refer to the void arrow head of drawing 1 (b)) is applied to the transition layer 29, stress concentration is not produced. Therefore, the crack of the passivation film 28 can be avoided and the characteristic effectiveness that the dependability of electronic parts 25 can be raised is acquired.
[0022]
In addition, although the transition layer 29 which has the height dimension Hb almost equivalent to the height dimension of the core substrate 23 was made into the example with the gestalt of the above-mentioned operation, it is not limited to this. For example, it is good also as thin film-like transition layer 29b which has height dimension Hb' smaller than Hb for whether your being Haruka (refer to drawing 6 (a)). What is necessary is to form the Bahia hall 45 and just to connect between the Bahia hall 31 (to refer to drawing 1 (a)) of the upper layer, and the die pads 27 of electronic parts 25 to the insulating resin layer 44 which carried out the laminating on that transition layer 29b through this Bahia hall 45 and thin film-like transition layer 29b, when it does in this way.
[0023]
Moreover, although the transition layer 29 (or 29b) is directly formed on the die pad 27 of electronic parts 25 in the above example, on both sides of the electric conduction film, you may form indirectly in between. That is, you may make it the structure of a die pad 27/the electric conduction film / transition layer 29 (or 29b). In this case, as electric conduction film, it can choose from copper, gold, silver, tin, chromium, titanium, nickel, zinc, cobalt, etc. Moreover, a spatter or plating can perform formation of the electric conduction film, and thickness of the electric conduction film can be set to 0.01-1.0 micrometers.
[0024]
[Effect of the Invention]
Since the path of a transition layer is set up more greatly than the diameter of opening of the passivation film which covers the periphery of a pad smaller than the path of a pad according to this invention, the angle of a transition layer is not located on a pad. For this reason, even if the passivation film is under a transition layer, it is not concerned with stress (force generated in the time of a resin press etc.) from a top, but the crack initiation of the passivation film and the structural members (Si etc.) under it can be avoided. Moreover, by carrying out roughening processing of the front face of a transition layer, association with insulating resin can be strengthened and peeling etc. can be avoided.
[Brief Description of the Drawings]
[Drawing 1] It is the sectional view (a) and its important section expanded sectional view (b) of the electronic-parts built-in multilayer substrate in the gestalt of operation.
[Drawing 2] It is the production process Fig. (the 1) of the electronic parts in the gestalt of operation.
[Drawing 3] It is the production process Fig. (the 2) of the electronic parts in the gestalt of operation.
[Drawing 4] It is the production process Fig. (the 3) of the electronic parts in the gestalt of operation.

[Drawing 5] It is the production process Fig. (the 4) of the electronic parts in the gestalt of operation.
[Drawing 6] It is the important section expanded sectional view showing the modification of the electronic-parts built-in multilayer substrate in the gestalt of operation.
[Drawing 7] They are the sectional view (a) showing an example of the conventional electronic-parts built-in multilayer substrate, and its important section expanded sectional view (b).
[Description of Notations]
21 Electronic-Parts Built-in Multilayer Substrate
24 Cavity
25 Electronic Parts
27 Die Pad (Pad)
28 Passivation Film
29 Transition Layer
31 Bahia Hall
32 Conductor -- Circuit (Wiring Layer)

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1]
In the electronic-parts built-in substrate possessing the electronic parts laid under the resin layer, the transition layer formed on the pad of these electronic parts, the passivation film which covers said pad, the Bahia hall formed on said transition layer, and the wiring layer connected to said transition layer through this Bahia hall,
The electronic-parts built-in multilayer substrate characterized by setting up more greatly [in the path (Dd) of said transition layer, it is smaller than the path (De) of said pad, and] than the diameter of opening of the passivation film which covers said pad (Df).
[Claim 2]
Said transition layer is an electronic-parts built-in multilayer substrate according to claim 1 characterized by having the roughening section in the contact surface with said resin layer.
[Claim 3]
In the electronic-parts built-in substrate possessing the electronic parts laid under the resin layer, the transition layer formed on the pad of these electronic parts, the passivation film which covers said pad, the Bahia hall formed on said transition layer, and the wiring layer connected to said transition layer through this Bahia hall,
The electronic-parts built-in multilayer substrate characterized by having the roughening section in the contact surface with said resin layer while setting up the path of said transition layer smaller than the diameter of opening of the passivation film which covers said pad.

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DESCRIPTION OF DRAWINGS

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25 Electronic Parts
27 Die Pad (Pad)
28 Passivation Film
29 Transition Layer
31 Bahia Hall
32 Conductor -- Circuit (Wiring Layer)

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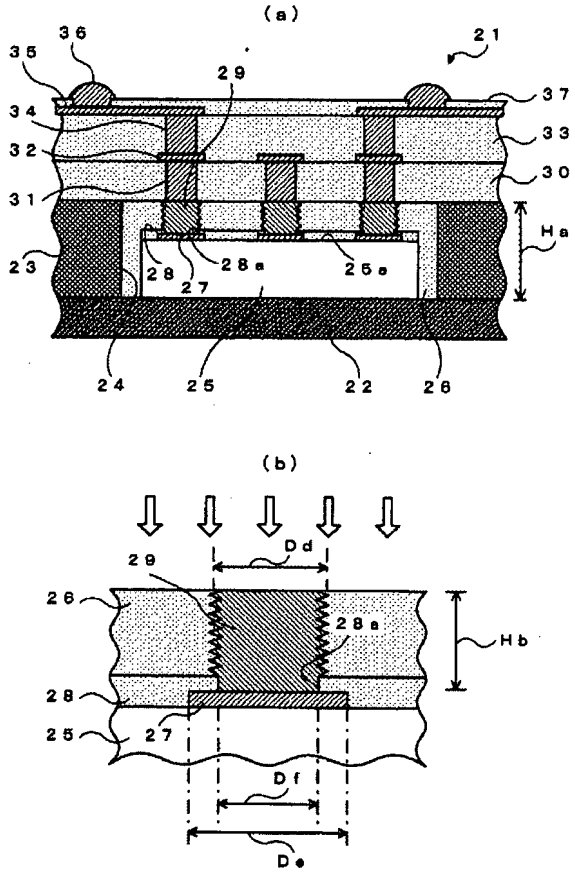
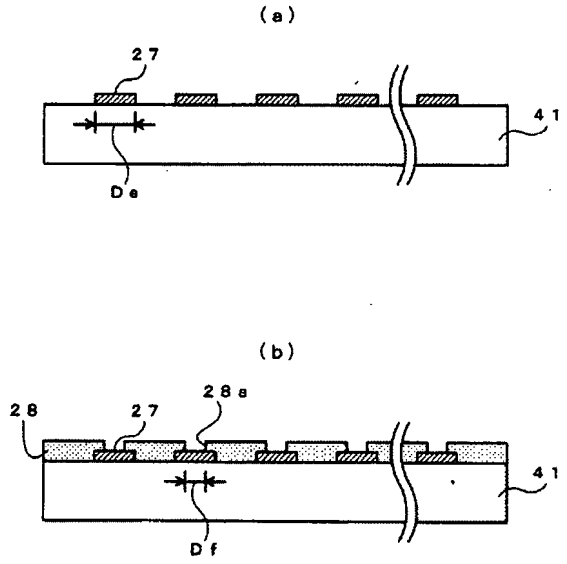
DRAWINGS

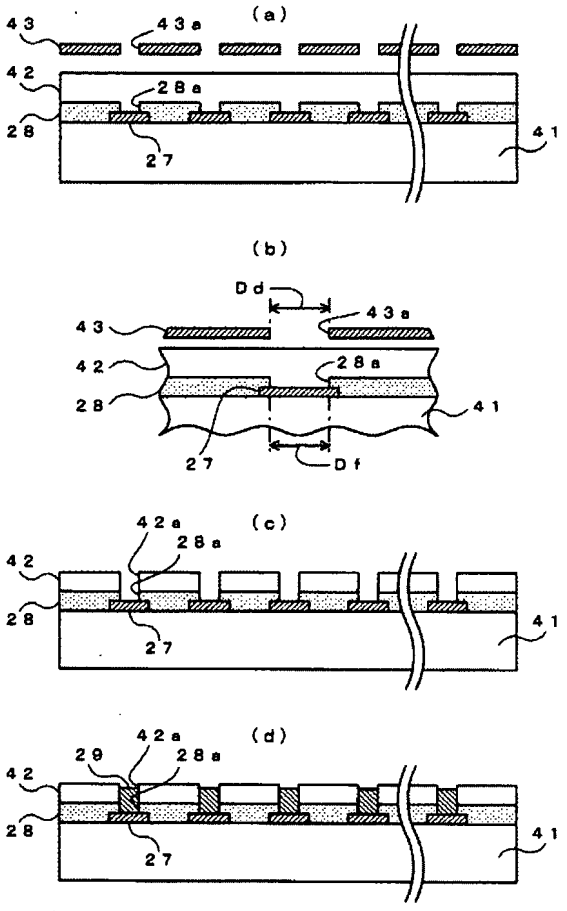
[Drawing 1]



[Drawing 2]


(a)
27
41
De
(b)
28
27
28a
41
Df

[Drawing 3]


(a)
43
43a
42
28a
28
27
41
(b)
Dd
43
43a
42
28a
28
41
27
Df
(c)
42a
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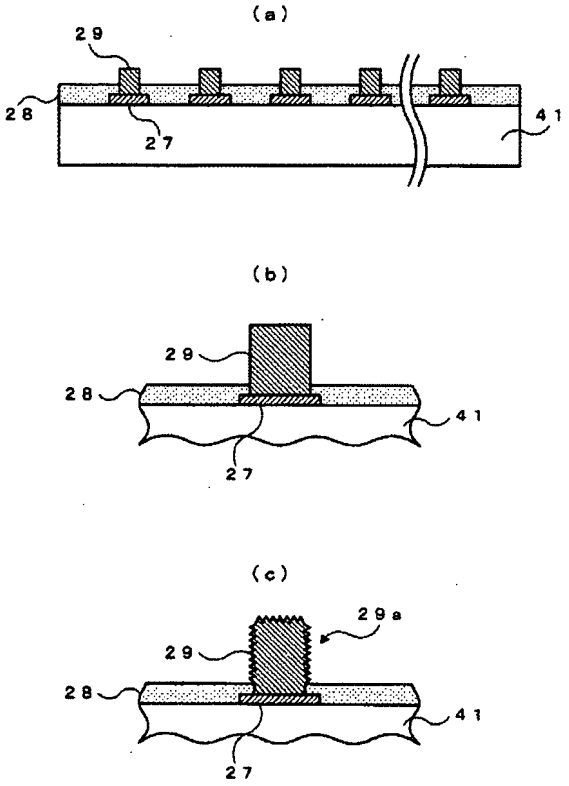
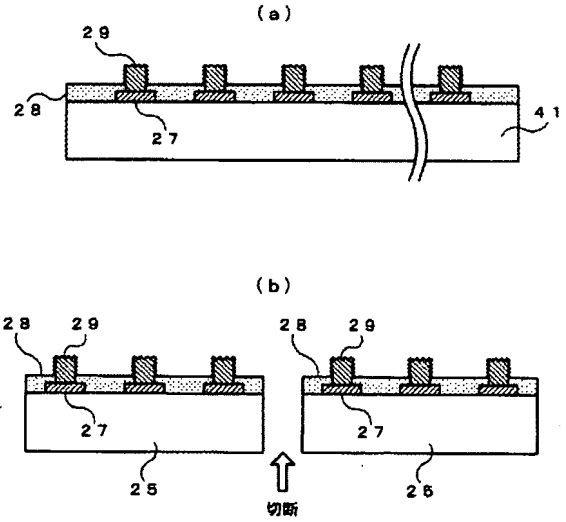
(d)
42a
29
28a
42
28
27
41

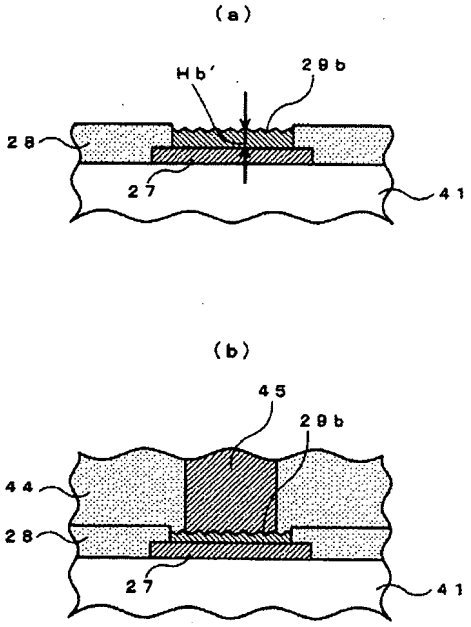
[Drawing 4]



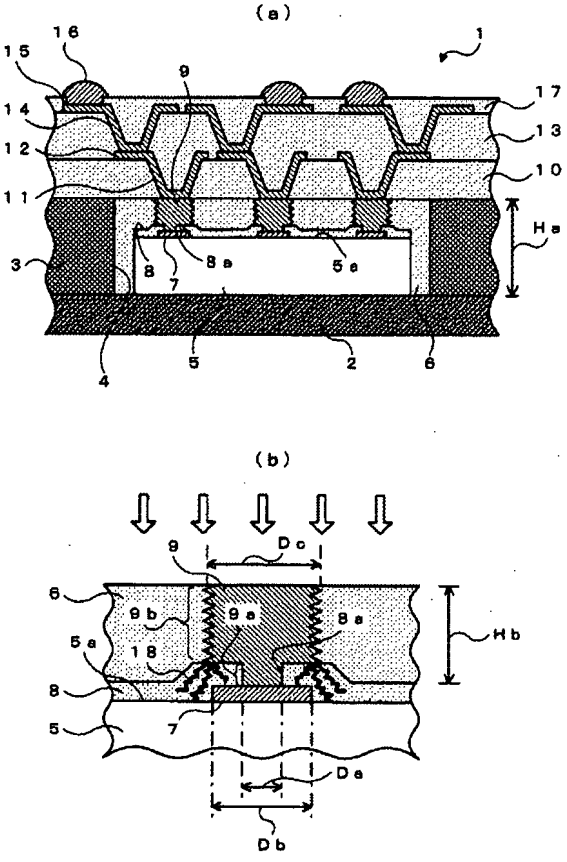
[Drawing 5]



[Drawing 6]



[Drawing 7]



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